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09/883,681	06/18/2001	Ashok Singhal	M-8496 US	1044

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EXAMINER	
PATEL, NIMESH G	

ART UNIT	PAPER NUMBER
2112	

DATE MAILED: 12/23/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/883,681	SINGHAL ET AL.	
	Examiner	Art Unit	
	Nimesh G Patel	2112	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *04 October 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-16 and 18-32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-16 and 18-32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 June 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *20041004*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on October 4, 2004 has been entered.

Claim Objections

2. Claims 19-27 are objected to because of the following informalities: The term "controller node" should be replaced by "node controller." Appropriate correction is required.

3. Claim 32 is objected to because of the following informalities: The term "data storage devices" should be replaced by "data storage device." Appropriate correction is required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

5. Claims 1, 3-16, 28-30, and 32 are rejected under 35 U.S.C. 102(b) as being anticipated by Cohen('464).

6. Regarding claim 1, Cohen discloses a node controller(Figure 1, 18) for a node in a data storage system having at least two nodes(Node 1:CPU 14 and Memory Controller 18A, Node 2 :CPU 16 and Memory Controller 18; Node 3: Memory Controller 18, Network Controller 26, Storage Controller 28, etc., Node 4:Memory Controller 18, Display Controller, etc.) the node

controller being distinct from a computer-memory complex of the node(Column 3, Lines 10-12; CPU has a cache and therefore is a computer-memory complex, i.e. processing system), the node controller being operable to transfer data between the two nodes as instructed by the computer-memory complex but without any further intervention by the computer-memory complex(Column 3, Lines 22-25 and 48-49).

7. Regarding claim 28, Cohen discloses a node controller, wherein the node controller comprises a logic engine operable to perform a logic operation on data from at least one data source in the data storage system(Column 6, Lines 5-7; Figure 3, 56; It is inherent an address comparator performs logic operations on address data).

8. Regarding claim 3, Cohen discloses a node controller, wherein at least one data source is one of an interconnect link, a peripheral component interconnect (PCI) bus, or a cluster memory(Figure 1).

9. Regarding claim 4, Cohen discloses a node controller, wherein the logic engine comprises an exclusive OR engine(Column 6, Lines 5-7; Figure 3, 56; It is inherent that address comparators use exclusive OR engines, as evidenced by Malinowski('441)).

10. Regarding claim 5, Cohen discloses a node controller comprising a command queue operable to store a logic control block to be processed by the logic engine(address comparator), the logic control block(transaction) specifying said at least one data source(Column 5, Lines 24-43; The address specifies the data source).

11. Regarding claim 6, Cohen discloses a node controller comprising a memory controller(Figure 3, 58) operable to interface with a cluster memory(Figure 1, 20).

12. Regarding claim 7, Cohen discloses a node controller, wherein the node controller is implemented as an integrated circuit device(Figure 1, 18).

13. Regarding claim 8, Cohen discloses a node controller comprising a peripheral component interconnect (PCI) control interface operable to support an interface between the node controller and a PCI bus(Column 5, Lines 13-23).

14. Regarding claim 9, Cohen discloses a node controller for transferring data through a node of a data storage system, the node controller being distinct from a computer-memory complex of the node(Column 3, Lines 10-12; CPU has a cache and therefore is a computer-memory complex, i.e. processing system), the node controller comprising: a plurality of logic engines operable to perform a logic operation on data from at least one data source in the data storage system(Column 6, Lines 5-7; Figure 3, 56; It is inherent the address comparator performs logic operations on the address data) and command queues coupled to the logic engines, the command queues operable to store logic control blocks which can be processed by the logic engines(Column 5, Lines 24-43).

15. Regarding claim 10, Cohen discloses a node controller wherein the at least one data source is one of an interconnect link, a peripheral component interconnect (PCI) bus, or a cluster memory(Figure 1).

16. Regarding claim 11, Cohen discloses a node controller, wherein at least one of the logic engines comprises an exclusive OR engine(Column 6, Lines 5-7; Figure 3, 56; It is inherent that address comparators use exclusive OR engines, as evidenced by Malinowski('441)).

17. Regarding claim 12, Cohen discloses a node controller comprising a memory controller(Figure 3, 58) operable to interface with a cluster memory(Figure 1, 20).

18. Regarding claim 13, Cohen discloses a node controller, wherein the node controller is implemented as an integrated circuit device(Figure 1, 18).

19. Regarding claim 14, Cohen discloses a node controller a peripheral component interconnect (PCI) control interface operable to support an interface between the node controller and a PCI bus(Column 5, Lines 13-23).

20. Regarding claim 15, Cohen discloses a node controller wherein the node controller is operable to be programmed by the computer-memory complex(the computer-memory complex would have to initialize the node controller and therefore would have to "program" the controller).

21. Regarding claim 16, Cohen discloses a producer register operable to specify a first address of a command queue and a consumer register operable to specify a second address of a command queue (Column 5, Lines 24-43).

22. Regarding claim 29, Cohen discloses a node controller for a first node in a data storage system comprising at least the first node and a second node(Node 1:CPU 14 and Memory Controller 18A, Node 2 :CPU 16 and Memory Controller 18; Node 3: Memory Controller 18, Network Controller 26, Storage Controller 28, etc., Node 4:Memory Controller 18, Display Controller, etc.), the node controller being distinct from a computer-memory complex of the first node(Column 3, Lines 10-12; CPU has a cache and therefore is a computer-memory complex, i.e. processing system), the node controller comprising: a memory controller(Figure 3, 58) for accessing a cache memory of the first node; one or more bus interfaces for communicating with a host device, a data storage device, and the computer-memory complex all located on one or more buses; a link to a second node(Figures 1 and 3; Column 5, Lines 21-23); wherein in a first type of data transfer: the computer-memory complex instructs the data storage device to write data into the memory; the data storage device writes the data into the memory via one or more buses; the computer-memory complex instructs the node controller to send the data to the

second node; and the node controller sends the data to the second node via the link(Column 3, Lines 48-62).

23. Regarding claim 30, Cohen discloses a node controller, further comprising: a logic engine; wherein in a second type of data transfer: the computer-memory complex instructs the node controller to perform a logic operation to a plurality of data in the memory; the node controller uses the logic engine to perform the logic operation to the plurality of data(Column 6, Lines 5-7; Figure 3, 56; It is inherent an address comparator performs logic operations on address data).

24. Regarding claim 32, Cohen discloses a node controller; wherein in a third type of transfer: the computer-memory complex instructs the data storage device to write the data into the memory; the data storage device writes the data into the memory via the one or more buses; the computer-memory complex instructs the host device to read the data from the memory; and the host device reads the data form the memory via the one or more buses(Column 3, Lines 48-62).

25. Claims 1, 9, 18 and 29 are rejected under 35 U.S.C. 102(b) as being anticipated by Williams et al.('038), hereinafter referred to as Williams.

26. Regarding claim 1, Williams discloses a node controller(Figure 1, 16) for a node in a data storage system having at least two nodes(Figure 1) the node controller being distinct from a computer-memory complex of the node(Figure 1, 12 and 22), the node controller being operable to transfer data between the two nodes as instructed by the computer-memory complex but without any further intervention by the computer-memory complex(Column 3, Lines 44-47 and 60-65).

27. Regarding claim 9, Williams discloses a node controller(Figure 1, 16) for transferring data through a node of a data storage system, the node controller being distinct from a

computer-memory complex of the node(Figure 1, 12 and 22), the node controller comprising: a plurality of logic engines operable to perform a logic operation on data from at least one data source in the data storage system(Column 5, Lines 46-49) and command queues coupled to the logic engines, the command queues operable to store logic control blocks which can be processed by the logic engines(Column 5, Lines 7-13).

28. Regarding claim 18, Williams discloses a node controller(Figure 1, 16) for transferring data through a node in a data storage system, the node controller comprising: a memory controller(Column 3, Lines 48-53; Column 4, Lines 2-13) for coupling to memory and a backplane, wherein the backplane can be coupled to a plurality of other node controllers in the data storage system(It is inherent for modern systems to have backplanes to connect devices); a plurality of input/output interfaces for coupling to a computer-memory complex of the node and a plurality of buses(Figure 1; Column 3, Lines 56-60), the plurality of input/output interfaces being coupled to the memory controller; where in the buses are coupled to a computer-memory complex of the node and each bus can be coupled to a plurality of devices(Figure 1); a plurality of logic engines coupled to (1) the memory controller and (2) the backplane(Column 5, Lines 46-49); wherein in a first type of data transfer, one of the logic engines performs a logic operation to a plurality of data from one of a plurality of data sources and writes the result of the logic operation to one of a plurality of data destinations, the data sources comprising the memory and the input/output interfaces, and the data destinations comprising, the memory, the backplane, and the input/output interfaces(Figure 1; Column 5, Lines 46-49).

29. Regarding claim 29, Williams discloses a node controller(Figure 1, 16) for a first node in a data storage system comprising at least the first node and a second node(Figure 1), the node controller being distinct from a computer-memory complex of the first node(Figure 1, 12 and 22), the node controller comprising: a memory controller for accessing a cache memory of the first

node(Column 4, Lines 2-13); one or more bus interfaces for communicating with a host device, a data storage device, and the computer-memory complex all located on one or more buses; a link to a second node(Figure 1; Column 3, Lines 56-60); wherein in a first type of data transfer: the computer-memory complex instructs the data storage device to write data into the memory; the data storage device writes the data into the memory via one or more buses; the computer-memory complex instructs the node controller to send the data to the second node; and the node controller sends the data to the second node via the link(Column 3, Lines 35-65).

Claim Rejections - 35 USC § 103

30. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

31. This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

32. Claims 18-27 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Cohen, in view of Styczinski('860).

33. Regarding claim 18, Cohen discloses a node controller for transferring data through a node in a data storage system, the node controller comprising: a memory controller(Figure 3,

58) for coupling to memory and a backplane, wherein the backplane can be coupled to a plurality of other node controllers in the data storage system(It is inherent for modern systems to have backplanes to connect devices); a plurality of input/output interfaces for coupling to a computer-memory complex of the node and a plurality of buses(Column 3, Lines 10-12; CPU has a cache and therefore is a computer-memory complex, i.e. processing system), the plurality of input/output interfaces being coupled to the memory controller; where in the buses are coupled to a computer-memory complex of the node and each bus can be coupled to a plurality of devices(Figures 1 and 3; Column 5, Lines 21-23); a plurality of logic engines coupled to (1) the memory controller and (2) the backplane(Column 6, Lines 5-7; Figure 3, 56; It is inherent the address comparator performs logic operations on the address data); and data sources comprising the memory and the input/output interfaces, data destinations comprising, the memory, the backplane, and the input/output interfaces(Figure 1).

Cohen does not specifically disclose wherein in a first type of data transfer, one of the logic engines performs a logic operation to a plurality of data from one of a plurality of data sources and writes the result of the logic operation to one of a plurality of data destinations. However, Styczinski discloses a node controller wherein one of the logic engines performs a logic operation to a plurality of data from one of a plurality of data sources and writes the result of the logic operation to one of a plurality of data destinations(Column 8, Line 48-Column 9, Line 10). Therefore, it would have been obvious to one of ordinary skill in the art to perform logic operations on the data from one of the data sources to one of the data destinations, as disclosed by Styczinski, since this would allow Cohen's system to operate a parity protected data storage.

34. Regarding claim 19, Styczinski discloses a node controller, wherein, in a second type of data transfer, one of the data sources(Figure 1, 101) writes a data into the memory and in

response one of the logic engine copies the data to at least one of the data destinations(Figure 1, 105)(Column 8, Line 48-Column 9, Line 10).

35. Regarding claim 20, Styczinski discloses a node controller, wherein each of the devices is selected from the group consisting of a host device(Figure 1, 101) and a data storage device(Figure 1, 105).

36. Regarding claim 21, Cohen discloses a node controller, wherein each of the input/output interfaces comprises a peripheral component interconnect(PCI) controller and each of the buses comprises a PCI bus(Figure 1, 36).

37. Regarding claim 22, Styczinski discloses a node controller, wherein the computer-memory complex mages the PCI bus(It is inherent the PCI bus is managed by the computer-memory complex).

38. Regarding claim 23, Cohen and Styczinski do not specifically disclose a node controller wherein the computer-memory complex supports a service selected from the group consisting of a HTTP service, a NFS service, and a CIFS service. Examiner is taking official notice that these services are well-known in the art(HTTP is used for internet, NFS is a standard used for providing file system mounts among Unix systems, and CFSI is the new proposed standard for an Internet File System) and would be obvious to use the computer-memory complex for such services since these services use a network of computers or nodes.

39. Regarding claim 24, Cohen discloses a node controller, wherein the computer-memory complex is not burdened with temporarily storing data being transferred thorough the node in the computer-memory complex(Column 3, Lines 22-25 and 48-49).

40. Regarding claim 25, Styczinski discloses a node controller, wherein the logic operation comprises an XOR operation(Column 5, Lines 35-38).

41. Regarding claim 26, Styczinski discloses a node controller, wherein the XOR operation is used to calculate a parity data for writing a full or a partial RAID stripe(Column 5, Lines 35-38).

42. Regarding claim 27, Styczinski discloses a node controller, wherein the XOR operation is used to reconstruct a lost data using a parity(Column 5, Lines 35-38).

43. Regarding claim 31, Cohen does not specifically disclose a node controller, wherein the second type of data transfer further comprises: the computer-memory complex instructs the node controller to send a result of the logic operation to the second node; and the node controller sends the result to the second node via the link. However, Styczinski discloses a node controller wherein one of the logic engines performs a logic operation to a plurality of data from one of a plurality of data sources and writes the result of the logic operation to one of a plurality of data destinations(Column 8, Line 48-Column 9, Line 10). Therefore, it would have been obvious to one of ordinary skill in the art to perform logic operations on the data from one of the data sources to one of the data destinations, as disclosed by Styczinski, since this would allow Cohen's system to operate a parity protected data storage.

Response t Arguments

44. Applicant's arguments filed October 4, 2004 have been fully considered but they are not persuasive. Applicant argues that Cohen does not disclose any element that corresponds to a node controller that is distinct from a computer-memory complex. However, Cohen does disclose a node controller(Figure 1; memory controller; each memory controller in Figure 1 corresponds to the claimed node controller of the applicant. The nodes corresponding to the each of the node controllers(i.e. memory controllers) are Node 1:CPU 14 and Memory Controller 18A, Node 2 :CPU 16 and Memory Controller 18; Node 3: Memory Controller 18, Network Controller 26, Storage Controller 28, etc., Node 4:Memory Controller 18, Display Controller, etc.) that is distinct from a computer-memory complex(Column 3, Lines 10-12; CPU has a cache and therefore is a computer-memory complex, i.e. processing system). Therefore, applicant's arguments are not persuasive.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nimesh G Patel whose telephone number is 571-272-3640. The examiner can normally be reached on M-F, 8:30-6:00.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 571-272-3632. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Nimesh G Patel
Examiner
Art Unit 2112

NP NP
December 10, 2004

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